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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/696,366	10/25/2000	Randal N. Linden	1005/203	3221

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EXAMINER	
PHAN, THAI Q	
ART UNIT	**PAPER NUMBER**
2128	4

DATE MAILED: 01/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/696,366	Randal Linden
Examiner	**Art Unit**
Thai Phan	2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct. 24, 2003* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) *4* is/are allowed.

6) ☒ Claim(s) *1-3 and 5-7* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Nov. 26, 2003* is/are a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☒ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☒ Interview Summary (PTO-413) Paper No(s). *05*
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to applicant's amendment filed on Oct. 24, 2003. Claims 5-7 are newly added. Claims 1-7 are pending in this Office Action.

Drawings

1. Formal drawings filed on Nov. 26, 2003 have been accepted.

Claim Rejections - 35 USC § 112

2. Due to amendment to the claim, the 35 USC 112 rejection has been withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blasciak, Andrew, US patent no. 5,103,394 in view of Bershteyn et al., US patent no. 5,678,028.

As per claim 1, Blasciak discloses a method and system for emulating execution of program instruction codes designed for a target system in a host with feature limitations

substantially similar to the claimed invention (Abstract and Summary of the Invention). According to Blasciak, the emulation method includes steps of

measuring execution speed of the target system in execution of the program instructions and a host system in emulation of target program (col. 4, lines 3-57, col. 5, lines 20-35, Figs. 12, 13, col. 10, lines 10-66, col. 17, lines 1-18)

measuring execution speed difference between the host processor and the target processor (Fig. 12, col. 10, lines 25-40, col. 11, line 52 to col. 12, line 54, cols. 13-18),

and configuring or reconfiguring the host system in order to conform to the execution speed of the target system in execution of the target program (cols. 12-18) for emulation or debugging process (Background of the Invention). Blasciak does not expressly disclose dynamically adjusting the execution speed of the host system to conform to target system as claimed. Such claimed feature is well known in the art. In fact, Bershteyn teaches a method and system for emulation. The system manages simulation or emulation speed of the host system (col. 4, lines 25-41). The system measures the speed difference or variance between the host system and the target CPU to adjust simulation time or execution speed of simulation host (Fig. 10, col. 9, line 47 to col. 10, line 7, for example) to eliminate unnecessary response time in the simulation process.

Practitioner in the art at the time of the invention was made would have found it obvious to modify Blasciak system by adjusting execution speed of the simulation host as taught in Bershteyn to speed up simulation time and eliminate response time for unnecessary events in instruction execution.

As per claim 2, Blasciak discloses identifying a block of instructions and associated processing time required by the target system (col. 5, lines 20-35, line 55 to col. 6, line 31, for example), determining real time required to execute by the target system (col. 6, lines 34-44, for example), and the time difference make to conform with the target system as claimed.

As per claim 3, Blasciak discloses measurement of speed of execution for program instruction blocks as claimed. Blasciak does not disclose adjusting speed of execution based on variance determined for a preceding block as claimed. Such feature is however well-known in the art. In fact, Bershteyn teaches a method and system for managing simulation or emulation speed of the host system (col. 4, lines 25-41). The system measures the speed difference or variance between the host system and the target CPU to adjust simulation time or execution speed of simulation host (Fig. 10, col. 9, line 47 to col. 10, line 7, for example) based on speed variance due to hardware differences between the host and target system in execution of simulation program to eliminate unnecessary response time in the simulation process.

Practitioner in the art at the time of the invention was made would have found it obvious to modify Blasciak system by adjusting execution speed of the simulation host as taught in Bershteyn to speed up simulation time and eliminate response time for unnecessary events in instruction execution.

As per claims 5 and 7, Bershteyn teaches execution speed of the host and the target system in emulation process as claimed.

As per claim 6, Bershteyn teaches adjusting execution speed of the host system in emulation of the target program by decreasing the speed of emulation execution by the host system as claimed.

Allowable Subject Matter

5. Claim 4 is allowed. The following is a statement of reasons for the indication of allowable subject matter:

Claim 4 requires the distinct features of by selecting a reference determined by an arbitrary time quantum of the execution speed, tracking the instruction cycles executed, determining an elapsed time period by querying a timing source, and determining a timing reference by comparing the elapsed time with the time quantum. The prior art of record does not show such distinct features as claimed to simulate the operating speed of the target system. Claim 4 is deemed allowable.

Response to Arguments

6. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

In response to applicant's argument Blasciak does not expressly disclose dynamically adjusting the execution speed of the host system to conform to the speed of the target system (page 6), the examiner agrees with. Such argued feature is however known in the art. Bershteyn teaches a method and system for managing simulation or emulation speed of the host system (col.

4, lines 25-41). The system measures the speed difference or variance between the host system and the target CPU in the emulation process as discloses in Blasciak to adjust simulation time or execution speed of simulation host as taught in Bershteyn (Fig. 10, col. 9, line 47 to col. 10, line 7, for example) to eliminate unnecessary response time in the simulation process.

Practitioner in the art at the time of the invention was made would have found it obvious to modify Blasciak system by adjusting execution speed of the simulation host as taught in Bershteyn to speed up simulation time and eliminate response time for unnecessary events in instruction execution.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this action should be mailed to:

Commissioner for Patents

P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for formal communications intended for entry)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

January 5, 2004

Thaiphan
Thai Phan
Patent Examiner
AU: 2128